

CPLD Development Kit - Xilinx - XC9572XL



Introduction and Features:

- The CPLD Development kit based on Xilinx XC9572XL is a low cost evaluation platform for training, testing and developing designs based on the Xilinx 9500XL family of CPLD.
- The board contains the 1600 gate, 72 macro cells, 100 Pin XC9572XL CPLD with 72 user I/O's.
- An on-board power supply includes 3.3V regulator, which regulates Vcc internal & Vcc I/O for the CPLD.
- A 25 MHz Crystal Oscillator provides clock source that is directly connected to GCK1 clock input on the 9572XL device.
- All user I/O pins are brought out of the 9572XL device.
- Peripheral interfaces like LEDs, 7 Segment Displays, Key Switches and Buzzer are provided on board.
- Separate Jumper settings have been provided for accessing the I/Os for other external applications.
- A built-in JTAG programmer board is also available for programming the XC9572XL.
- The HDL code can easily be implemented using the Webpack software available on the Xilinx Website.
- Datasheets are provided in the CD-ROM accompanying the Kit and a softcopy of the user manual is also included in the CD as well.

Contents of XC9572XL Development Kit:



The CPLD Development Kit consists of the following:

- CPLD Development Board (Main PCB) mounted on plastic enclosure.
- Xilinx - XC9572XL Daughter Board fixed on the Main PCB.
- Parallel Port Cable for programming through built-in JTAG Port.
- Power Cord.
- CD ROM with Software, example VHDL codes and User Manual.

Specifications:

- On board regulated power supply 3.3V
- XC9572XL CPLD–100 Pins, 1600 Gates, 72 Macro Cells & 72 User I/O
- 25 MHZ Four Pin Crystal Oscillator
- Built-in JTAG Programmer
- Parallel port connector for JTAG Programming
- 2 X 7 Segment Display
- 4 X 4 Tact Key Switches
- 16 LED Indicators
- 2 X 8 Slide Switches
- Buzzer
- Jumper Selectable Port Pin
- External I/O Port Pins
- Universal Switch Mode Power Supply input 100V to 240V AC, 0.40A, 47-63 HZ, 15-Watts maximum.

VLSI DESIGN LAB

The following experiments are possible to simulate using VHDL and verified experimentally in the CPLD Development Kit – Xilinx – XC9572XL offered by Winnii.

No.	Details of Experiments
1.	Gates
2.	D flip-Flop 7474
3.	Decade Counter – 7493
4.	4 Bit Counter – 7493
5.	Shift Registers – 7495
6.	Universal Shift Registers – 74194 / 195
7.	3 to 8 Decoder – 74138
8.	4 Bit Comparator – 7485
9.	8 X 1 Multiplexer – 74151
10.	16 X 1 Multiplexer – 74150

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